IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Rajesh Sundaram, et al.	§	Group Art Unit:	2827
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APPEAL BRIEF

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Stephanie Petreas

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 014711/0143.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1, 3-5, 7, 9, 22-25, 27-30, 32 and 33 stand rejected. Claims 10-11, 14-17, 19, 31, 35-36 and 38 have been allowed. Claims 2, 6-8, 12-13, 18, 20-21, 26, 34 and 37 have been cancelled.

Enclosed herewith is an amendment that cancels claims 1, 3-5 and 9 and places claim 7 in independent form. The rejection of pending claims 7, 22-25, 27-30, 32 and 33 are being appealed.

IV. STATUS OF AMENDMENTS

Appellants filed a "Reply to Final Office Action Mailed August 15, 2006" on September 29, 2006. In an Advisory Action dated October 20, 2006, the Examiner indicated that the amendment would not be entered.

Enclosed herewith is an Amendment Filed With Appeal Brief Under 37 C.F.R. §41.33 that cancels claims 1, 3-5 and 9 and places claim 7 in independent form.

V. SUMMARY OF CLAIMED SUBJECT MATTER

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

Independent claim 7 is a method claim. Support for claim 7 may be found, for example, in the specification at page 6, lines 3-13 and page 10, lines 6-11.

Independent claim 22 is an independent system claim. Support for independent claim 22 may be found, for example at specification at page 6, lines 3-13; page 10, lines 6-11; and page 17, lines 15-26.

Referring now to FIG. 1, shown is a schematic diagram of a memory array in accordance with one embodiment of the present invention. As shown in FIG. 1, memory array 100 includes a plurality of memory cells formed at the intersections of wordlines (e.g., WL_n) and bitlines (e.g., BL_n). Wordlines may also be referred to as address lines, in certain embodiments. Each memory cell includes a control or select gate and a floating gate. As shown in FIG. 1, each memory cell has a select gate coupled to a wordline, and a terminal or electrode coupled to a bitline and another terminal or electrode coupled to a source line. In such manner, each memory cell is uniquely addressable via a selected wordline and bitline (i.e., row and column). Specification, p. 3, ln. 18 - p.4, ln. 5.

In the embodiment of FIG. 1, memory cell 110_n, for example, includes a drain terminal coupled to bitline BL_n, a select gate coupled to wordline WL_n, and a source terminal coupled to a common source line (shown in FIG. 1 as coupled to ground (GND)). Specification, p. 4, lns. 11-15.

As shown in FIG. 1, wordline WL_n is selected for programming. A wordline may be selected for programming by providing a high voltage signal to the wordline. Further shown in FIG. 1, during a programming activity a bitline is selected (e.g., BL_n), and is provided with a voltage. For example, in a programming operation for a MLC, a selected bitline may be provided with a voltage between approximately 4-7 volts. In the embodiment shown in FIG. 1, bitline BL_n may be provided with a voltage of approximately 5 volts. In such manner, the drain terminal of selected memory cell 110_n is biased between approximately 4-7 volts. Because the selected bitline is taken to a high voltage, deselected memory cells (e.g., 112_n and 114_n) also

connected to the selected bitline also see the high voltage that couples to the wordlines of deselected cells, causing the IDTO leakage (shown in FIG. 1 as a bold arrow extending down bitline BL_n). Specification, p. 5, ln. 6 – p. 6, ln. 2.

When wordline WL_n is selected for programming, other wordlines, including wordlines WL_{n-1} and WL_{n-2} shown in FIG. 1 are deselected. In various embodiments of the present invention, such deselected wordlines may be provided with a negative voltage during certain portions of erasing and programming activities. For example, a negative voltage may be applied during erase operations, such as preconditioning and pulse conditioning, in addition to programming activities. In such manner, leakage in deselected memory cells coupled to a selected bitline may be reduced. Specification, p. 6, lns. 3-13.

Referring now to FIG. 2, shown is a schematic diagram of control circuitry in accordance with one embodiment of the present invention. As shown in FIG. 2, control circuitry 200 may be used to provide a desired negative voltage to one or more deselected wordlines of a memory array. As shown in FIG. 2, a negative charge pump 210 may include a negative pump 212 and a switch 214. Switch 214 may be controlled via signals from additional control circuitry (not shown in FIG. 2). Negative pump 210 may be used to supply a negative voltage to a NDR mode select switch 220. In one embodiment, two control signals, ldnpmpen and ldneg1sw may be used to determine a desired output from negative pump 210. Specifically, in one embodiment if the ldnpmpen signal is a logic low, the switch 214 is open and a ground potential is present. Alternately, if the ldnpmpen signal is a logic high and the ldneg1sw switch is a logic low, a -8 volt signal may be output from negative pump 210. When both control signals are logic high, a -4 volt signal may be output from negative pump 210. As shown in FIG. 2, a negative voltage of -4 volts may be supplied by negative pump 210 as HNEGPMP. Specification, p. 6, ln. 22 – p. 7, ln. 19.

Further shown in FIG. 2 is NDR mode switch 220, which may be used to generate desired negative voltages for biasing decoders and deselected wordlines coupled thereto. NDR mode switch 220 may operate generally as a voltage divider to provide multiple negative voltages. As shown in FIG. 2, NDR mode switch 220 is coupled to receive the HNEGPMP signal from negative pump 210. In the embodiment of FIG. 2, NDR switch 220 may include an inverter 221, a depleted mode N-channel transistor 222 and four triple well N-type transistors (223-226) coupled in series. As shown in FIG. 2, transistor 222 has a gate terminal coupled to

receive signal hlref133s from additional control circuitry, a source terminal coupled to an output of inverter 221 and a drain terminal coupled to a drain terminal of transistor 223. Specification, p. 7, ln. 22 – p. 8, ln. 13.

As further shown in FIG. 2, each of transistors 223-226 has a drain terminal coupled to its gate terminal and a source terminal coupled to the substrate of the respective transistor. In such manner, when inverter 221 is enabled by the ldneg1sw signal, and the hlref133s signal turns on transistor 222, NDR mode switch 220 may generate a first negative voltage at node 227 and a second negative voltage at node 228. In the embodiment of FIG. 2, first negative voltage may be a -1 volt signal (HNPMP) and second negative voltage may be a -3 volt signal (HN3PMP). Specification, p. 8, lns. 14-23.

As further shown in FIG. 2, the first and second negative voltages from NDR mode switch 220 are provided to a negative switch 230, more specifically, to a voltage level shifter 232 and voltage level shifter 234. Level shifters 232 and 234 may be controlled by a signal (ldvnxl) from the additional control circuitry such that the level shifters output the first and second negative voltages when the ldvnxl signal is active and a ground potential when ldvnxl is inactive. Specification, p. 9, lns. 16-24.

Still referring to FIG. 2, for each wordline of the memory array, an x-decoder 240 may be present. Such a decoder may be used to provide the desired negative voltage to a deselected wordline with which it is associated, while also being capable of providing a high voltage programming pulse when the wordline is selected for programming. Specifically, x-decoder 240 may include a triple well n-channel transistor M0 coupled such that the second negative voltage may bias a P-well of the transistor. When so biased and an associated wordline 260 is deselected, transistor M0 passes the first negative voltage signal onto deselected wordline 260. In the embodiment of FIG. 2, this negative voltage is a -1 volt signal. Specification, p. 10, lns. 6-18.

More so, similar circuitry present in x-decoder circuitry of all other deselected wordlines of a given block of a memory array may supply a negative voltage to its corresponding wordline. However, at the same time, an x-decoder of a selected wordline may be biased such that the corresponding n-channel transistor M0 for the selected wordline is not even partially turned on. That is, for the selected wordline, the corresponding M0 transistor may be maintained off so that it does not pull down the wordline voltage of the selected wordline. As further shown in FIG. 2,

x-decoder 240 includes a P-type transistor 247 having a drain terminal coupled in series with a drain terminal of transistor M0 at node 248. The gate terminals of transistors M0 and transistor 247 are coupled together, and a source terminal of transistor 247 is coupled to signal HHVPX. Collectively, transistors 247 and M0 may act as a driver for wordline 260. X-decoder 240 also includes pre-driver circuitry to provide a programming pulse and other voltages desired for other operations of the memory cell. More specifically, x-decoder 240 includes a P-type transistor 241 having a source terminal coupled to signal HHVPIX and a gate terminal coupled to HHAWL. Further, the source terminal of transistor 241 is coupled to the substrate of the transistor. A drain terminal of transistor 241 is coupled in series to four n-type transistors 242-245. At one end of the transistor chain, the source terminal of transistor 245 is coupled to ground. Specification, p. 10, ln. 19 – p. 11, ln. 20.

As further shown in FIG. 2, intermediate node 246 is coupled between the drain terminal of transistor 241 and the drain terminal of transistor 242 and is further coupled to the gate terminals of transistors M0 and 247. In accordance with the embodiment of FIG. 2, for a selected wordline transistors 242-245 may have select signals enabled such that intermediate node 246 is provided a path to ground. Thus for a selected x-decoder 240, with intermediate node 246 at a ground potential, transistor 247 is turned on to pass a programming pulse HHVPX onto wordline 260, and transistor M0 is turned off. Specification, p. 12, lns. 1-11.

For a deselected x-decoder 240, at least one of transistors 242-245 will not be selected and thus a path to ground is not established. Accordingly, when transistor 241 is enabled via an active HHAWL signal, the voltage HHVPIX is passed onto intermediate node 246. In certain embodiments, the voltage of the HHVPIX signal may be between approximately 4-5 volts. In such manner, transistor M0 is turned on to pass the first negative voltage onto wordline 260, while transistor 247 is turned off. Wordline 260 is coupled to a select gate of transistor 255 of a memory cell 250. Further shown in FIG. 2 is a +5 volt signal applied to a drain terminal of transistor 255. Such a 5 volt signal may be used to provide desired biasing for a programming operation of memory cell 250. Specification, p. 12 – p. 13, ln. 4.

In various embodiments, all deselected wordlines of a memory device may be provided with a negative voltage. In such manner, IDTO leakage may be reduced, thereby reducing intrinsic charge loss (ICL) by 200 millivolts. In other embodiments, deselected wordlines may be taken to a negative voltage greater than -1 volt. While such negative voltages may vary, in

certain embodiments a negative voltage of between approximately -1 volt to -3 volts may be effected. In still further embodiments, greater negative voltages may be supplied. For example, by applying a greater negative voltage at the P-well of transistor M0, its threshold voltage (V_T) may be further raised and an even greater negative voltage may be passed to deselected wordlines.

Thus in many embodiments, it is desirable to provide a second negative voltage to the substrate of transistor M0 in order to raise its V_T such that for a selected x-decoder 240, transistor M0 is not partially turned on, while for deselected x-decoders a greater negative voltage may be passed to associated wordlines. For example, if no -3 volt signal were applied to the substrate of transistor M0, and the gate of M0 was at approximately ground as for a selected cell, if the HNVNX signal applied to the source terminal of M0 was any voltage greater than the threshold voltage (e.g., more negative than approximately -0.7 volts in the embodiment of FIG. 2), the device would start to turn on, causing both p-transistor 247 and n-transistor M0 to be active, pulling down the wordline voltage of the selected cell. Instead, by providing a second negative voltage to the substrate of transistor M0 via the HNVNPWX signal, the V_T of the transistor may be raised to approximately 1.3 volts (if HNVNPWX is at -3 volts). In such manner, a -1 volt HNVNX signal applied to the source terminal of transistor M0 does not cause the transistor to turn on, even if its gate terminal is at approximately ground potential. Specification, p. 13, ln. 5 – p. 14, ln. 14.

FIG. 3 is a block diagram of a representative data processing system, namely computer system 300 with which embodiments of the invention may be used. In one embodiment, computer system 300 includes a processor 310. The processor 310 may be coupled over a host bus 315 to a memory hub (i.e., a memory controller) 330 in one embodiment, which may be coupled to a system memory 320 via a memory bus 325. The memory hub 330 may also be coupled over an Advanced Graphics Port (AGP) bus 333 to a video controller 335, which may be coupled to a display 337.

The memory hub 330 may also be coupled (via a hub link 338) to an input/output (I/O) hub 340 that is coupled to a input/output (I/O) expansion bus 342 and a Peripheral Component Interconnect (PCI) bus 344. The I/O expansion bus 342 may be coupled to an I/O controller 346 that controls access to one or more I/O devices. As shown in FIG. 3, these devices may include in one embodiment storage devices, such as a floppy disk drive 350 and input devices, such as

keyboard 352 and mouse 354. The I/O hub 340 may also be coupled to, for example, a hard disk drive 356 as shown in FIG. 3. The PCI bus 344 may be coupled to various components including, for example, a flash memory 360 which may include the structures shown in the schematic diagrams of FIGS. 1 and 2. Further shown in FIG. 3 is a wireless interface 362 coupled to the PCI bus 344, which may be used in certain embodiments to communicate with remote devices. Specification, p. 15, ln. 19 – p. 17, ln.26.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Each of the following grounds of rejection are presented for review:

(1) claim 7 stands rejected under 35 U.S.C. §102(b) over Gill;

(2) claims 22-24, 28 and 30 stand rejected under 35 U.S.C. §102(e) over Gill;

(3) claim 25 stands rejected under 35 U.S.C. §102(e) over Gill;

(4) claim 27 stands rejected under 35 U.S.C. §102(e) over Gill;

(5) claim 29 stands rejected under 35 U.S.C. §102(e) over Gill;

(6) claim 32 stands rejected under 35 U.S.C. §102(e) over Gill;

(7) claim 33 stands rejected under 35 U.S.C. §§102(e) over Gill.

VII. ARGUMENT

(1) Claim 7 Is Patentable Under 35 U.S.C. §102(b) over Gill

Claim 7 is a method claim that recites supplying a negative voltage to at least one deselected wordline from a decoder coupled to the deselected wordline during programming on a selected wordline, providing the negative voltage and a control negative voltage to the decoder, where the control negative voltage is provided to a substrate of a transistor of the decoder that is coupled to pass the negative voltage to the deselected wordline.

Pending claim 7 stands rejected under 35 U.S.C. §102(e) over U.S. Patent No. 5,537,362 (Gill). The rejection is improper. As contended support for teaching supplying a negative voltage to at least one deselected wordline during a programming operation on a selected wordline, the Examiner refers solely to the abstract of Gill for such a teaching. However, all that Gill teaches is that *during a read operation*, a negative voltage is provided to deselected wordlines. However, Gill never teaches or suggests supplying such a negative voltage during a programming operation. In fact, Gill plainly teaches the opposite. That is, as shown in Table 1 of Gill, during a programming (i.e., write) operation, a ground voltage is supplied to deselected wordlines, not a negative voltage. Instead, as shown in Table 1, the only time a negative voltage is provided to deselected wordlines is during a read operation.

The rejection of claim 7 is further improper, as Gill certainly nowhere teaches providing a control negative voltage to a substrate of a transistor of a decoder. As contended support for this recited subject matter, the Examiner refers to column 8, lines 63-67. However, all that this portion of Gill teaches is that a voltage regulator includes two p-type CMOS transistors 62. Nowhere, however does Gill anywhere teach that a control negative voltage is provided to a substrate of either of these transistors. Nor is this voltage regulator 36 of Gill a decoder, as recited by claim 7. Accordingly, claim 7 is patentable and the rejection should be reversed.

(2) Claims 22-24, 28 and 30 Are Patentable Under 35 U.S.C. §102(e) over Gill

Claim 22 recites a non-volatile memory array and a decoder coupled to the non-volatile memory array to supply a negative voltage to a deselected wordline of the array, where the decoder includes a first transistor of a first polarity to pass the negative voltage to the deselected wordline and a second transistor of a second polarity to pass a program voltage if the deselected

wordline becomes a selected wordline. Claim 22 further recites a wireless interface coupled to the non-volatile memory array. Claim 22 stands rejected under 35 U.S.C. § 102(e) over Gill.

Gill nowhere teaches a decoder that includes a first transistor of a first polarity to pass a negative voltage to a deselected wordline and a second transistor of a second polarity coupled to the first transistor to pass a program voltage. In this regard, the Examiner refers to FIG. 5 of Gill, and more specifically to multiple pMOSFETs 62. However, both of these MOSFETs are of a single polarity. Furthermore, these MOSFETs are not even of a decoder. Instead, these transistors of Gill are part of a voltage regulator that receives a signal from a decoder. Gill, col. 8, lns. 5-21. However, they are not part of the decoder itself. Furthermore, these transistors of Gill do not pass a negative voltage if the wordline is deselected for programming and instead a program voltage if the wordline is selected for programming.

The rejection of claim 22 is further improper, as there is no basis for contending that the recited wireless interface coupled to a non-volatile memory is somehow inherent in the system of Gill. "In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily flows* from the teachings of the applied prior art." *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added). That is, to meet the inherency requirement, Gill must *necessarily* require a wireless interface coupled to a non-volatile memory. As the Examiner concedes that such an interface is "optional," (Final Office Action, p. 5) inherency cannot be established and the rejection is overcome. That is, the concession by the Examiner that such a wireless interface is "optional" utterly defeats any contention that this wireless interface "necessarily" be present. As such, this anticipation rejection of claim 22 is improper and the rejection of claim 22 and the claims depending therefrom should be reversed.

(3) Claim 25 Is Patentable Under 35 U.S.C. §102(e) over Gill

Claim 25 depends from claim 22 and further recites that the first transistor includes a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage and a drain terminal coupled to pass the negative voltage to the deselected wordline. Claim 25 stands rejected under 35 U.S.C. § 102(e) over Gill. The rejection is improper at least for the same reason discussed above regarding claim 22 (*see* VII.2).

The rejection is further improper, as the Examiner simply refers to the voltage regulator 36 of Gill, discussed above which shows two p-type transistors 62. Neither of these transistors are disclosed to include a well that are coupled to receive a negative control voltage. Nor do either of these transistors include a drain terminal coupled to pass a negative voltage to the deselected wordline. Instead, all that Gill teaches is that "the voltage regulator circuit 36 [that] can be used to regulate the voltage applied to a single wordline 14 by the wordline address decoder 32 ...." Gill, 8:4-7.

(4) Claim 27 Is Patentable Under 35 U.S.C. §102(e) over Gill

Claim 27 depends from claim 22 and further recites a pre-driver circuit to disable the first transistor of the decoder if the deselected wordline becomes a selected wordline, where the pre-driver circuit includes a transistor chain coupled to an intermediate node coupled to a gate of the first transistor. Claim 27 stand rejected under 35 U.S.C. § 102(e) over Gill. This rejection is improper at least for the same reason discussed above regarding claim 22 (*see* VII.2).

The rejection is further improper, as all that the Examiner contends to support the rejection is again a voltage regulator 36 and the p-type transistors 62. However, neither of these transistors is a transistor chain that is coupled to an intermediate node coupled to a gate terminal of the transistors. Instead, as shown in FIG. 5 of Gill, both of transistors 62 simply have gate terminals coupled to their source terminals. Nor does a ground potential disable either of these transistors, as these transistors are indicated as being p-type transistors (and thus are active when supplied a ground potential). Accordingly, the rejection of claim 27 should be reversed.

(5) Claim 29 Is Patentable Under 35 U.S.C. §102(e) over Gill

Claim 29 depends from claim 28 and further recites that the flash memory includes a multi-level cell flash memory. As contended support for this rejection, the Examiner refers to column 1, lines 24-35 of Gill, which in the background of Gill simply recites that flash EEPROMs include an array of memory cells. However, Gill nowhere teaches or suggests that its flash memory be a multi-level cell flash memory. Accordingly, for this further reason the rejection of claim 29 should be reversed.

(6) Claim 32 Is Patentable Under 35 U.S.C. §102(e) over Gill

Claim 32 depends from claim 22 and further recites a negative switch coupled to provide a negative voltage and a negative control voltage to a decoder. Claim 32 stands rejected under 35 U.S.C. §102(e) over Gill. This rejection is improper and should be reversed.

As contended support, the Examiner refers to a wordline address decoder 32 which includes a switch. However, Gill nowhere teaches that the switch is either a negative switch, or where the switch provides two voltages to a decoder. Instead, as clearly shown in FIG. 3 the voltages are not provided to a decoder, but out of a decoder and to a voltage regulator 36 and a capacitor 44. For these further reasons, the rejection of claim 32 is improper and should be reversed.

(7) Claim 33 Is Patentable Under 35 U.S.C. §102(e) over Gill

Claim 33 depends from claim 32 and further recites that the negative switch is coupled to further provide a negative voltage and the negative control voltage to a second decoder coupled to a different wordline. This rejection is improper for the same reasons discussed immediately above with regard to claim 32 (*see* VII.6).

The rejection is further improper as Gill nowhere teaches that this switch and a single wordline address decoder 32 is somehow provided to any other decoder. Instead, as taught by Gill, each voltage regulator circuit 36 and wordline address decoder 32 is used for each wordline 14. Gill, 8:5-12. Accordingly this switch within the wordline address decoder 32 of Gill is nowhere coupled to another decoder, and thus the rejection of claim 33 is further improper and should be reversed.

Appellants respectfully request that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

The claims on appeal are:

Claim 7: A method comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a programming operation on a selected wordline;

providing the negative voltage and a control negative voltage to the decoder, further comprising providing the control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline; and

supplying a positive voltage to the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage.

Claim 22: A system comprising:

a nonvolatile memory array having a plurality of memory cells each coupled to a wordline and a bitline;

a decoder coupled to the nonvolatile memory array to supply a negative voltage to a deselected wordline of the nonvolatile memory array, wherein the decoder comprises a first transistor of a first polarity to pass the negative voltage to the deselected wordline and a second transistor of a second polarity coupled to the first transistor to pass a program voltage, if the deselected wordline becomes a selected wordline; and

a wireless interface coupled to the nonvolatile memory array.

Claim 23: The system of claim 22, wherein the decoder is further coupled to supply a positive voltage to the deselected wordline if it becomes a selected wordline.

Claim 24: The system of claim 22, further comprising a second decoder to supply a positive voltage to a selected wordline while the negative voltage is supplied to the deselected wordline.

Claim 25: The system of claim 22, wherein the first transistor comprises a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected wordline.

Claim 27: The system of claim 22, further comprising a pre-driver circuit to disable the first transistor if the deselected wordline becomes a selected wordline, wherein the pre-driver circuit comprises a transistor chain coupled to an intermediate node coupled to a gate terminal of the first transistor, wherein the transistor chain is to provide a ground potential to the intermediate node to disable the first transistor.

Claim 28: The system of claim 22, wherein the nonvolatile memory array comprises a flash memory.

Claim 29: The system of claim 28, wherein the flash memory comprises a multi-level cell flash memory.

Claim 30: The system of claim 22, wherein the wireless interface comprises an antenna.

Claim 32: The system of claim 22, further comprising a negative switch coupled to provide the negative voltage and a negative control voltage to the decoder.

Claim 33: The system of claim 32, wherein the negative switch is coupled to further provide the negative voltage and the negative control voltage to a second decoder coupled to another wordline of the non-volatile memory array.

IX. EVIDENCE APPENDIX

There was no evidence submitted during prosecution.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings in this matter.